17.8 A 0.12µm CMOS Comparator Requiring 0.5V at 600MHz and 1.5V at 6GHz

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Flash ADCs contain many clocked regenerative comparators. The demands on these comparators are, therefore, that they consume little power, have high sampling rates, and have small areas. In [1] a 4GS/s 4b flash ADC in 0.18µm CMOS was presented, and comparators with 4 stages and integrated inductors were implemented. Such inductors usually need a large chip area. Typically, in ADCs pre-amplifiers are added before the comparator to enhance the resolution. Fast comparators are often designed in CML, where the differential design avoids common-mode disturbances. Whether or not the constant tail currents and the low voltage swings are beneficial depends on the intended application. In [2] a 10GHz 3-stage comparator in 0.11µm/1.2V CMOS was presented, which was used to extract every 4th bit of a 40Gb/s data stream. With $1V_{pp}$ at the input a BER < 10^{-12} was achieved. In [3] a comparator in 0.18µm/1.8V CMOS was described, it consumed 350µW at 1.4GHz. The standard deviation of the offset without compensation was σ = 31.6mV. One way to reduce power consumption is to lower the supply voltage. In [4] a 1b quantizer in 0.18µm CMOS for sub-1V ΔΣ modulators was presented. Simulations showed that with a 0.8V power supply the quantizer consumed 134µW at 10MHz. In [5] a latch-type sense amplifier in 0.13µm CMOS was described, which properly worked down to a supply voltage of 0.7V with a comparison time longer than 11ns.

The comparator presented here works down to a supply voltage of 0.5V with a maximum clock frequency of 600MHz and consumes 18µW. For a BER better than 10^{-9} a minimum input voltage difference of 60.5mV at 600MHz, or 25.8mV at 500MHz, or 21.2mV at 400MHz, has to be applied to the comparator. At a supply voltage of 1.5V these values are 38mV at 5.5GHz, 29.4mV at 5GHz, 16.5mV at 4GHz and 11.2mV at 3GHz. At 6GHz a BER of 10^{-6} is achieved with a 150mV difference. The comparator consumes 2.65mW at 1.5V/6GHz and 2.17mW at 1.5V/4GHz, which were measured at a separate supply pad. The output voltage swing is sufficient to drive a CMOS logic gate. According to Monte-Carlo simulations on 50 samples, the standard deviation of the comparator's offset is σ = 23mV at a supply voltage of 1.5V and σ = 57mV at 0.5V.

Figure 17.8.1 shows the schematic of the comparator. A clock cycle is divided into a reset and a comparison phase. In opposition to a conventional comparator, transistors P0 and P1 are used to reset the comparator when CLK is V_{SS} and when CLK changes to V_{COMP} the same transistors are biased as active loads. So additional reset switches, which contribute parasitic capacitances to the output nodes and reduce speed, are avoided. During the reset phase, CLK and CLKR are equal to V_{SS}, transistors N0 and N1 are switched off and transistors P0 and P1 are switched on and pull both output nodes OUT and $\overline{OUT}$ towards V_{Comp}. If CLK changes to V_{Comp}, transistors N0 and N1 are switched on. Because transistor N8, which has threshold voltage V_{tn8} and is biased with an adjustable voltage TBIAS at its gate, has been added to the clock line, CLKR rises to TBIAS - V_{tn8} (sub-threshold- and leakage currents are neglected for simplicity) and P0 and P1 are biased to become active loads. At the beginning of the comparison phase the output nodes are initially pre-charged to V_{Comp} from the previous reset. Transistors N6 and N7 are on and each of transistors N2 and N3 (latch) has an initial gate voltage near V_{Comp}. This fact, combined with the fact that N2 to N8 are transistors with threshold voltages of about 0.29V, which are provided by this CMOS process, makes it possible to drive the comparator even down to a supply voltage of 0.5V. The latch switches because of positive feedback that depends on the input-voltage difference (CINP-CINN) at transistors N4 and N5. To reduce static current flow after the comparator's decision is made, transistors N6 and N7 are added below transistors N4 and N5. When the voltage level at, for example, OUT is below the threshold voltage of N7, the path via N5 to $\overline{OUT}$ is cut off. At pin NWELL the separate n-well of P0 and P1 is biased.

The block diagram of the test chip with the comparator is shown in Fig. 17.8.2. The chip is divided into 2 parts, one with a supply voltage of V_{DD} = 1.5V for optimal functionality of the CMOS logic needed for measurement purposes, and a second (V_{Comp}) where the comparator is placed. The clock is applied to pin CLKIN and processed by the clock driver to 2 complementary rectangular clock signals CLK and $\overline{CLK}$ with logic levels V_{SS} and V_{Comp} respectively. RC low-pass filters are added for adjusting the clock duty-cycle to about 50% by varying the bias voltage at CLKIN. The adapters convert the logical levels V_{Comp} and V_{SS} to V_{DD} = 1.5V and V_{SS} respectively. When the comparator is reset the decision is held in the transfer stages. With a digital switch, controlled by pin DIG1, signals CLK or $\overline{CLK}$ could be checked at output CREF.

The schematic of the adapter with the following transfer stage is depicted in Fig. 17.8.3. After the buffer-inverter N9-P2, which is supplied by V_{COMP}, a differential amplifier compares the logic signal with a voltage LREF. The difference is amplified so that the resulting output voltages are compatible with the logic levels of the following inverter N12-P6, which is supplied by V_{DD}. LREF was adjusted from outside the chip. While the comparator is reset, switches P8 and N14 are closed and the previous decision is held dynamically at the input capacitance of the following buffer, which is directly placed after P8 and N14. The signal on digital pin DIG2 determines whether the transmission gate N15-P9 is always switched on, or is connected to the clock, where it is only switched on when transmission gate N14-P8 is off. In the second case, a constant overall delay time in relation to the clock is achieved to avoid having to adjust the optimal delay time in the BER analyzer for every measurement, because the comparator's decision time depends on several parameters, for example, the input voltage difference.

BER measurements were made by applying a bias voltage at CINP, which was superimposed with a 2^{31}-1 PRBS. Figure 17.8.4 shows a plot of the BER versus the bias level at CINP for different clock frequencies, supply voltages and amplitudes of PRBS 2^{31}-1. The amplitude is defined here by CINP - (CINN + offset) because CINN and CINP were biased separately during the measurements to compensate for the offset. It can be seen that every curve has a working point at a bias level of CINP, for example, 0.6V at 1.5V supply and 3GHz clock, where the BER is optimal. For fine-adjustment the bias voltage at NWELL can be lowered, which typically shifts this point to a higher input common-mode level.

Figure 17.8.5 shows some BER measurements versus the amplitude of PRBS 2^{31}-1 at the optimal working point for different parameters. To achieve a better BER, the input amplitude has to be raised, for example, more than 21.2mV is needed for a BER better than 10^{-9} at 0.5V and 400MHz.

Figure 17.8.6 shows oscilloscope pictures at a clock rate of 6GHz and in Fig. 17.8.7 a chip micrograph is shown. The size of the comparator is 22µm×21µm.

Acknowledgements:
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References:

[1] S. Park, Y. Palaskas and M. P. Flynn, "A 4GS/s 4b Flash ADC in 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 570-571, 2006.
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[4] M. Maymandi-Nejad and M. Sachdev, "1-Bit Quantiser with Rail to Rail Input Range for Sub-1V ΔΣ Modulators," *Electronics Letters*, pp. 894-895, June 12, 2003.
[5] B. Wicht, J.-Y. Larguier and D. Schmitt-Landsiedel, "A 1.5V 1.7ns 4k×32 SRAM with a Fully-Differential Auto-Power-Down Current Sense Amplifier," *ISSCC Dig. Tech. Papers*, pp. 462-463, 2003.

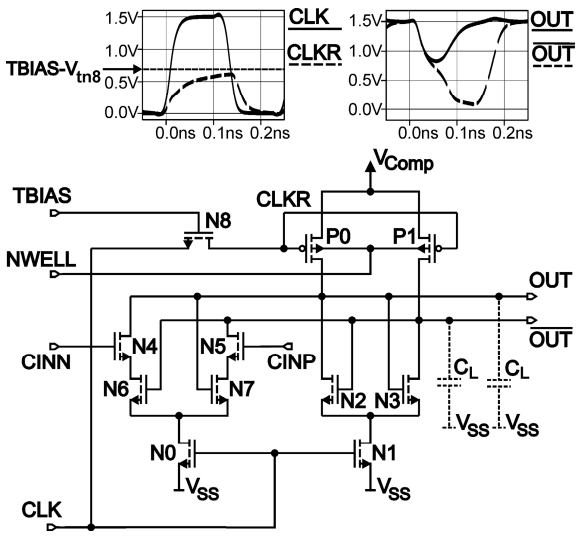

Figure 17.8.1: Comparator schematic.

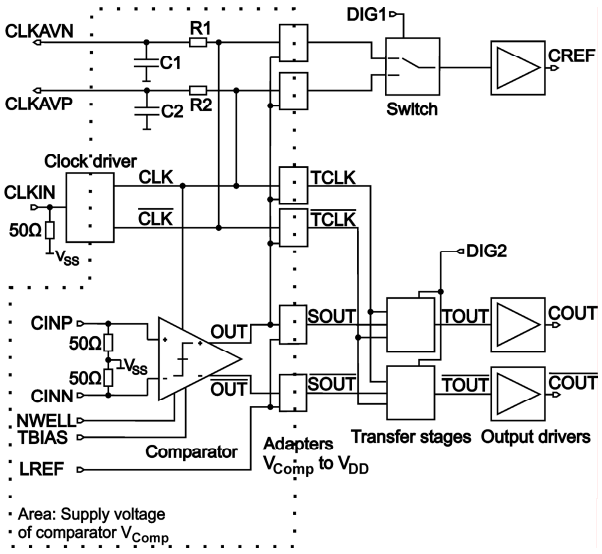

Figure 17.8.2: Block diagram of the test chip with the comparator.

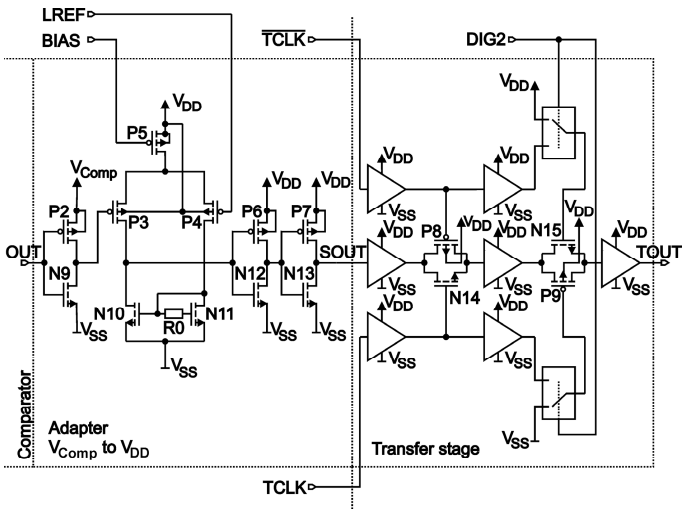

Figure 17.8.3: Simplified schematic of the adapter and the transfer stage.

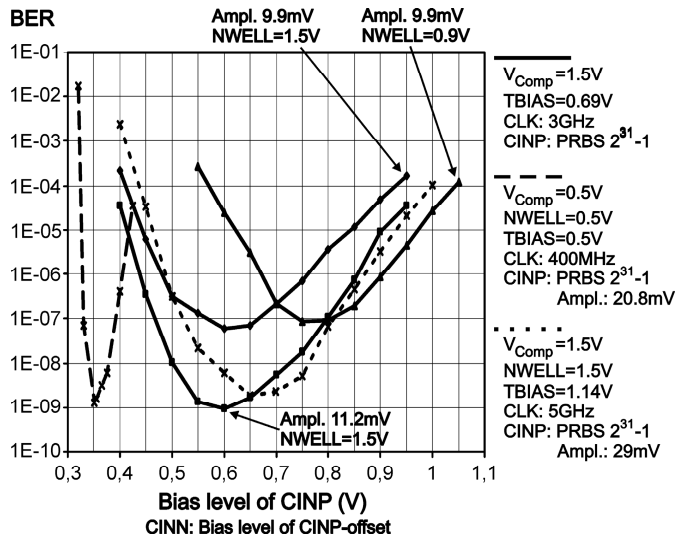

Figure 17.8.4: Bit error rate versus bias level at CINP.

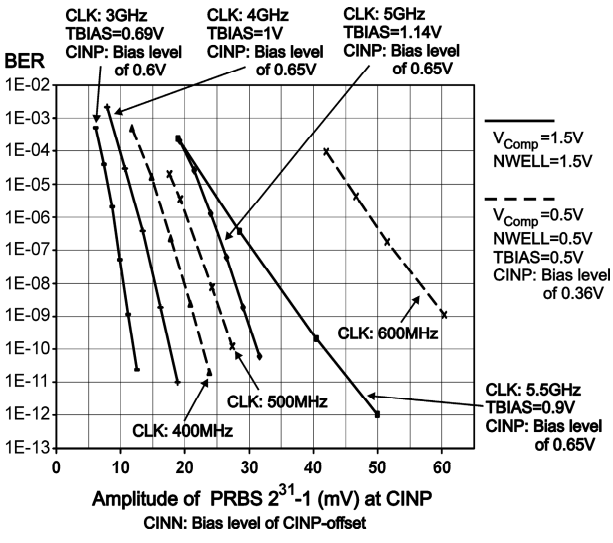

Figure 17.8.5: Bit error rate versus amplitude at CINP.

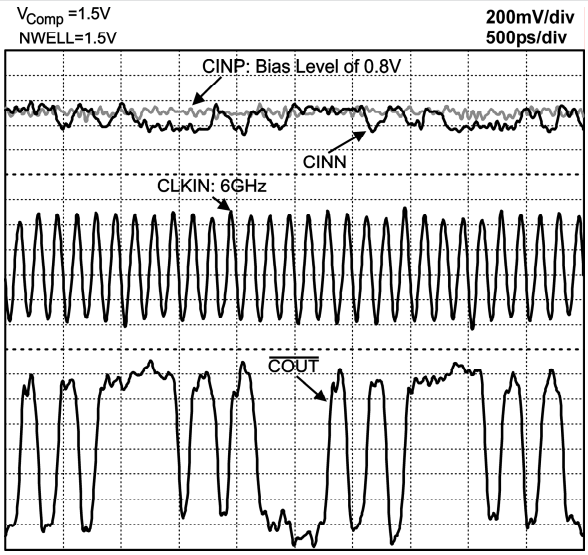

Figure 17.8.6: Oscilloscope pictures with a 6GHz clock.

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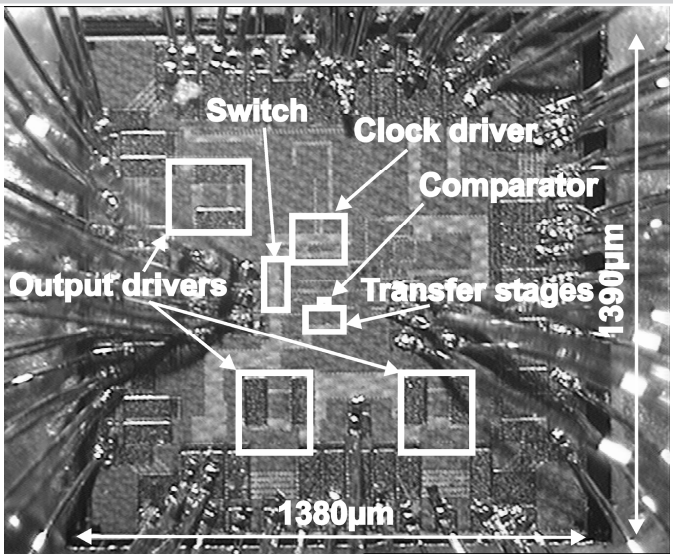

Figure 17.8.7: Micrograph of the test chip.

